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Comparison of the multi-gate functionality of screen-grid field effect transistors with finFETs

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Abstract
Two-dimensional (2D) technology computer-aided design (TCAD) is used to analyze and compare the multi-gate digital performance of the screen-grid field effect transistor (SGrFET) with a finFET. The switching speed of the all-n-type inverter is ten times faster for the n-SGrFET than for the n-finFET, while the noise margins are ∼400 mV for a 1 V supply for both devices. The performance of the complementary inverter is similar for both devices. The multi-gate functionality of both devices is exploited to minimize the device count for NAND, NOR and XOR gates. The SGrFET XOR contains only two devices while three are needed for the finFET. The rise time of the SGrFET logic gates is found to be almost half of that of the finFET. Complete OFF states can be obtained for the SGrFET via the multiple unit cell approach.

1. Introduction

As CMOS scales down with the aim of increasing operation speed and packing density, the need for better control of the channel by the gate has driven research toward devices with multiple gate configurations. Different types of multiple gate field effect transistors (FETs) have been proposed. The finFET with two, three or even four gate configurations is the most popular [1]. Symmetrical double-gated finFETs [2, 3] with two channels are considered in this work. The relationship between the geometrical parameters that optimize their performance [3] is

$$W_{\text{fin}} = \tfrac{1}{2}L_{\text{eff}} - 6t_{\text{ox}} \qquad W_{\text{fin}} > 2 \times h_{\text{fin}}, \tag{1}$$

with W_{fin} and h_{fin} being the fin width and height, respectively, and L_{eff} is the effective source–drain distance and t_{ox} is the oxide thickness.

The screen-grid field effect transistor (SGrFET) is an alternative multi-gate FET [4]. As the finFET, the SGrFET is defined on silicon-on-insulator (SOI). Its gating geometry is completely different as illustrated in figure 1(*b*). In contrast to the finFET, the SGrFET is planar. The gate consists of multiple cylindrical cavities with a thin thermal oxide sidewall and a poly-Si or metal filling. These gate cylinders (fingers) stand perpendicular to the current flow in the SOI body (channel). Different gate cavity configurations are possible [4]. In this work, we use the two-rows gate configuration. In figure 1(*b*), a 1-unit cell device is shown. To increase the current drive without impacting the performance parameters, the number of unit cells may be increased [4]. Note that in finFETs, a parallel connection of fins is used to increase current. Highly doped source and drain areas are located at both sides of the device and have the same width as the device, avoiding contacting problems to small areas. The channel doping is low to undoped in order to preserve high mobility values and is of the same doping type as the contact regions, unlike in traditional MOSFETs. The device operation is essentially MESFET-like. The role of the second row of gate fingers (near the drain) is to overcome the undesirable short channel effects. The SGrFET outperforms other MOSFET structures in the sub-threshold and weak inversion regions [5].

Figure 2 illustrates the differences in the gating action between the SGrFET and finFET. In finFETs, gating inverts a channel underneath the gate oxide at each side of the fin. In contrast, in SGrFETs the gates control the degree of carrier

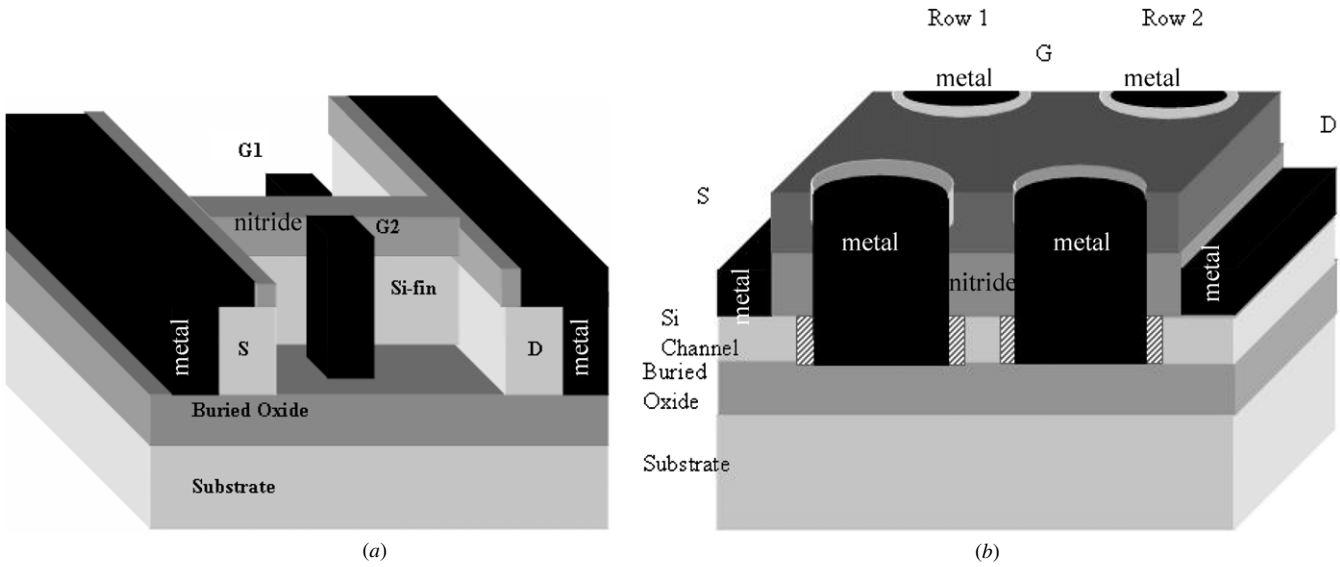


Figure 1. (*a*) Schematic configuration of a finFET with double gate configuration, G1: gate at the back and G2: gate in the front of the fin. (*b*) A schematic configuration of the SGrFET with two gating rows, each consisting of two half-gate cylinders. In this illustration, the top gate contact connects all gate cylinders in a single gate contact configuration. S is the source, D is the drain and G is the gate. Color coding: cross-hatched: SiO_2.

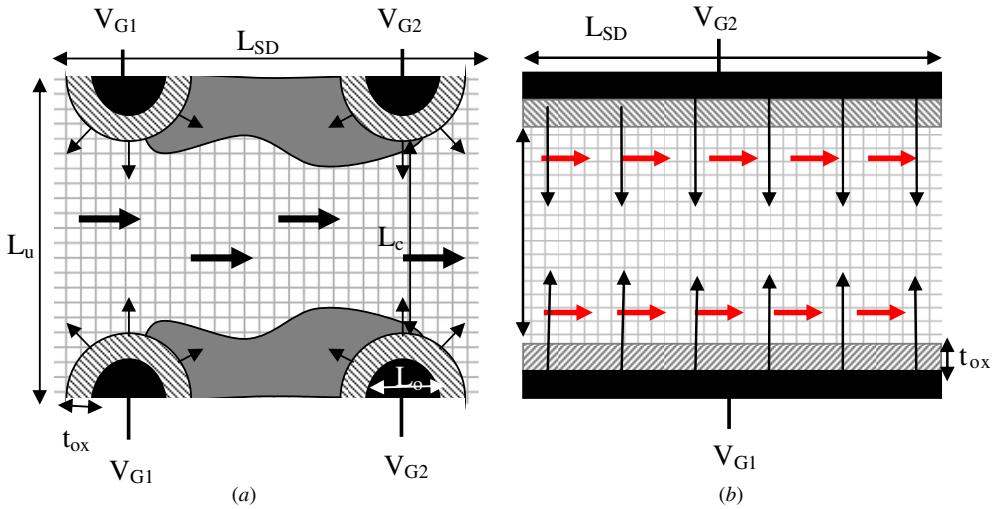


Figure 2. 2D cross-sectional view of the gating action in (*a*) SGrFET, (*b*) finFET. Black: gate contact, hashed: gate oxide, dark gray: depletion region, thin arrows: electric field caused by potential on the gate and fat arrows: current flow.

depletion between the gate cylinders. As a consequence, the carriers in the SGrFET travel away from the Si/SiO_2 interface, thus limiting surface roughness scattering and increasing mobility.

The threshold voltage (V_{th}) in both devices needs to be controlled via an appropriate choice of the gate work function. Table 1 gives V_{th} for two different gate metals for both FETs. An appropriate choice of gate material allows for both enhancement and depletion mode devices. This can be used for digital circuits using single carrier-type devices.

2D technology computer-aided design (TCAD) simulations are done in Medici^{TM} [6] on the cross-sectional plane from source to drain parallel to the wafer surface. The hydrodynamic (HD) model has been used for dc simulations as the length of the active region is under a quarter micron; nevertheless, the dc results obtained from drift-diffusion (DD) and HD models are similar. Therefore, the DD model was

Table 1. Device type and threshold voltage as a function of the work function with $|V_{DS}| = 1$ V.

Device type	V_{th} (V)	Metal work function (V)	Example of gate contact
n-SGrFET	0.38	4.8	Gold
p-SGrFET	−0.23	4.8	Gold
n-SGrFET	−0.2	4.10	Aluminum
n-finFET	0.39	4.8	Gold
p-finFET	−0.24	4.8	Gold
n-finFET	−0.35	4.10	Aluminum

used for the transient analysis in order to save CPU time and prevent convergence problems. The effective field and concentration-dependent mobility models are used for both devices.

The paper is organized as follows. In section 2, the dc performance of the SGrFET and finFET in both split-gate and normal-gate configurations is given. In section 3, four logic circuits with a minimized number of devices will be presented and the performance of the SGrFET and finFET logic gates will be compared. Discussions and conclusions are given in section 4.

2. DC analysis

In order to investigate the stable device functionality for digital applications, dc analysis of both finFET and SGrFET in a split-gate configuration is carried out. In a split-gate, the different gates are separated and can be biased individually. The split-gate configuration lends itself ideally for mixing and single device logic as synchronous or asynchronous voltages can be applied to the two gates [7]. Device physics of double-gate (DG) SOI MOSFETs, and their applicability to CMOS logic and memory has been studied in [8, 9].

For both finFET and SGrFET, the gate oxide thickness is $t_{ox} = 2$ nm and the source–drain distance $L_{SD} = 140$ nm. For the SGrFETs, the diameter of the gate cylinders is $L_O = 50$ nm. The gate diameter is an extra SGrFET parameter that can be used to control its operation. The distance between the outer oxide edges of the gate cylinders in the SGrFET within one row is $L_c = 50$ nm and L_u is the width of the device. L_c defines the effective width of the device and is taken equal to the width of the fin in the finFET (see figure 2). These geometrical parameters obey equation (1). The channel in both devices is undoped (10^{15} cm^{-3}); drain and source regions are highly doped (10^{19} cm^{-3}). In order to limit CPU time, 1-unit cell SGrFETs are used. N unit cells will give N times the current drive of 1-unit cell while all other performance parameters remain unaffected [4]. Thus, the total width of the unit cell in the simulations is $W_u = 2 \times L_O/2 + 2 \times t_{ox} + L_c = 104$ nm, unless otherwise stated and the width of the finFET is $W_u = 2 \times t_{ox} + L_c = 54$ nm, with $L_c = W_{fin} = 50$ nm. This makes the footprint of the finFET almost half of that of the SGrFET. Note, however, that this disadvantage disappears when using a parallel connection of fins as no gaps need to be left when connecting SGrFET unit cells [4].

Figure 3 shows the dc transfer characteristics for the split-gate n-SGrFET. In the simulations the voltage of one gate row is kept high ($H = 1$ V) or low ($L = -0.3$ V) while the voltage on the other gate row changes gradually between these two values. The source–drain voltage is kept at $V_{DS} = 1$ V.

For the finFETs, two different configurations are proposed in figure 4. One is the normal double-gate finFET and the other is a four-gate finFET similar to the four-gate SGrFET configuration. The dc transfer characteristics related to each device are shown in figure 5. The high–low voltages in the four-gate finFET are as in the SGrFET. Due to symmetry, only one gate in an L or H state is needed for the normal finFET. Table 2 gives a summary of the value of the threshold voltage

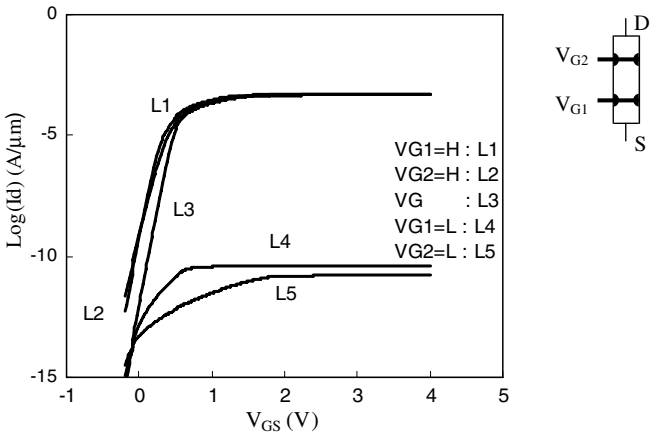


Figure 3. Transfer characteristics of the dc sweep of one gate row with the other gate row voltage constant. (L1) $V_{G1} = H$, V_{G2} swings; (L2) $V_{G2} = H$, V_{G1} swings; (L3) V_G swings (single gate contact configuration); (L4) $V_{G1} = L$ V_{G1} swings; (L5) $V_{G2} = L$, V_{G2} swings. $V_{DS} = 1$ V. H = high (1 V) and L = low (−0.3 V) gate voltage. Inset: gates V_{G1} and V_{G2} are as defined in figure 2.

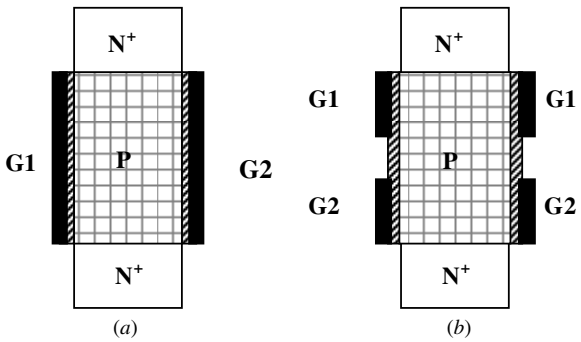


Figure 4. (*a*) Double-gate (normal) finFET. The fin width is the same for both finFETs. (*b*) Four-gate finFET similar to the SGrFET.

and sub-threshold slope in all studied cases. As expected, the on-current of the finFET is almost double that of the SGrFET.

For logic applications, we have chosen the values for the high and low gate voltages for which the device is respectively ON and OFF as in [10]:

$$V_{ON} = V_{DD} + V_{th}$$
$$V_{OFF} = -V_{th}. \qquad (2)$$

In the SGrFETs when one of the gate rows is kept at OFF, the drain current is very low ($I_{OFF} < 1.2 \times 10^{-13}$ A μm^{-1}) and the sub-threshold slope, S, is very high ($S > 158$ mV dec^{-1}). This is a result of the efficiency of the pinch-off of the channel with one single gate row. Opening of a part of the channel region by increasing the voltage on the other gate row does not allow the SGrFET to switch on. However, when one of the gate rows is ON, currents increase and S decreases to near-optimal values. The threshold voltage shifts between H and L states, creating the possibility for single device logic. In double-gate finFETs, by keeping one gate constant and swinging the other gate, the

Table 2. DC parameters of the double-gate SGrFET, double-gate (normal) finFET and four-gate finFET operations.

Device	Configuration	V_{th} (V)	S (mV dec^{-1})
Double-gate SGrFET	$V_{G-D} = H$, V_{G-S} swings	0.40	68.4
	$V_{G-D} = L$, V_{G-S} swing	0.16	158.2
	$V_{G-S} = H$, V_{G-D} swings	0.30	80.2
	$V_{G-S} = L$, V_{G-D} swings	0.17	186.9
	V_G swings	0.40	61.0
Four-gate finFET	V_{G1} swings $= H$, V_{G2} swings	0.17	101.3
	$V_{G1} = L$, V_{G2} swings	0.78	300.0
	$V_{G2} = H$, V_{G2} swings	0.24	93.7
	$V_{G2} = H$, V_{G2} swings	0.18	127.8
	V_G swings	0.35	67.8
Double-gate finFET	$V_{G1} = H$, V_{G2} swings	−11.35	14 537.0
	$V_{G1} = L$, V_{G2} swings	0.52	113.6
	V_G swings	0.39	63.8

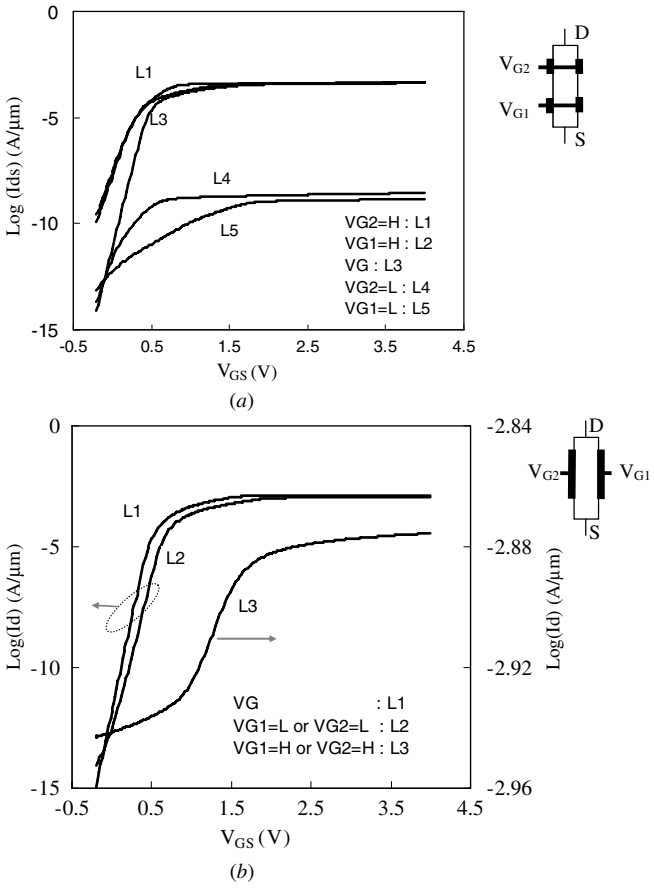


Figure 5. Transfer characteristics for (*a*) four-gate finFET—dc sweeps as in figure 4. (*b*) Normal finFET—dc sweep of one gate with the other gate voltage constant. $V_{DS} = 1$ V, $H =$ high (1 V) and $L =$ low (−0.3 V) gate voltage. Gates G_1 (=V_{G1}) and G_2 (=V_{G2}) are as defined in figure 4.

device threshold voltage changes more dramatically compared to the SGrFET but currents remain high and the sub-threshold slope also degrades. The four-gate finFET shows reduced performances compared to the SGrFET and normal finFET. This is due to the lack of gate control over the part of the channel where the gate is split. As a result, this four-gate configuration cannot be used to the same performance level as the SGrFET.

3. Logic circuit analysis

In this section, we first investigate SGrFET and finFET classical complementary and all-n-FET (enhancement–depletion, EDMOS) inverter circuits where both the SGrFET and finFET are used in a single gate bias configuration. Then the results of the analysis of NAND, NOR and XOR gates in which the split-gate configurations discussed in section 2 are exploited to make the circuit more compact will be given [6]. Both dc and transient analysis will be presented.

3.1. Inverter circuits

As stated above, two possible configurations are studied: the complementary C-FET and the n-EDMOS inverters. The ON and OFF gate voltages are respectively taken as $V_{ON} = 1$ V (−1 V) and $V_{OFF} = 0$ V for the n (p)-type FETs. The load in both n-EDMOS inverters is the depletion mode, with $V_{th} = -0.22$ V for the n-SGrFET and $V_{th} = -0.24$ V for the n-finFET. Thus, when the driver works in the linear region, the load is in its saturation region. The supply voltage, V_{DD}, is equal to 1 V in both inverters. The circuits are given in figure 6. The value of the capacitive load, C_L, is the input capacitance of the following stage (its value can be changed to accommodate the fan-out of a specific circuit). To estimate C_L in the SGrFET, we compose the oxide capacitances of the four half-gate cylinders (equation (3)) and for finFETs C_L is calculated based on the composition of two planar gate electrodes (equation (4)). These results are close to those extracted from ac simulations:

$$C_L = 2\varepsilon_{ox}\varepsilon_o \frac{(2\pi r_{in})}{t_{ox}} h \tag{3}$$

$$C_L = 2\varepsilon_{ox}\varepsilon_o \frac{L_g}{t_{ox}} h, \tag{4}$$

where ε_{ox} is the relative permittivity of the oxide, ε_0 is the permittivity of vacuum, h is the height of the Si channel, t_{ox} is the gate oxide thickness, r_{in} is the inner radius of the gate cylinder in the SGrFET and L_g is the gate length in the finFET. $C_L = 0.27$ fF and 0.24 fF for the SGrFET and finFET respectively.

Figure 7 shows the dc transfer characteristics of all inverter circuits. The C-FET for both SGrFET and finFET provides

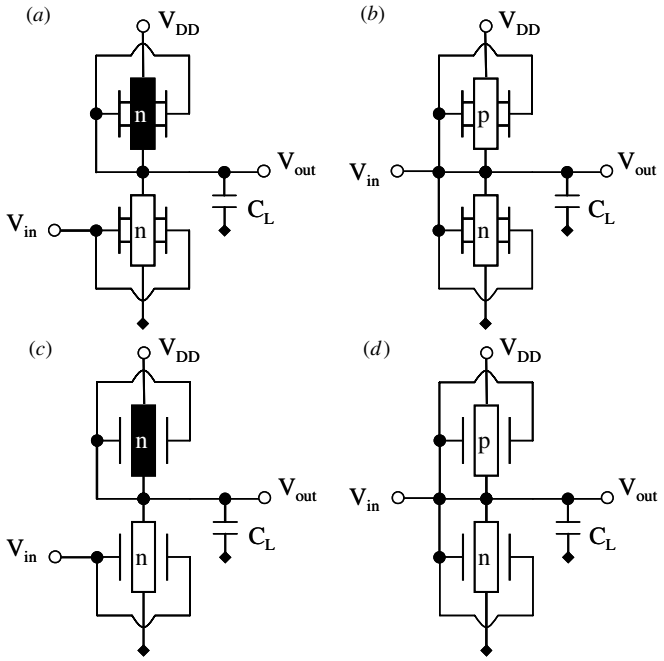


Figure 6. Definition of the device symbol and circuit. A full rectangle refers to the depletion mode. The symbol (n, p) in the rectangle defines the device type. (*a*) n-SGrFET inverter, (*b*) C-SGrFET inverter, (*c*) n-finFET inverter, (*d*) C-finFET inverter.

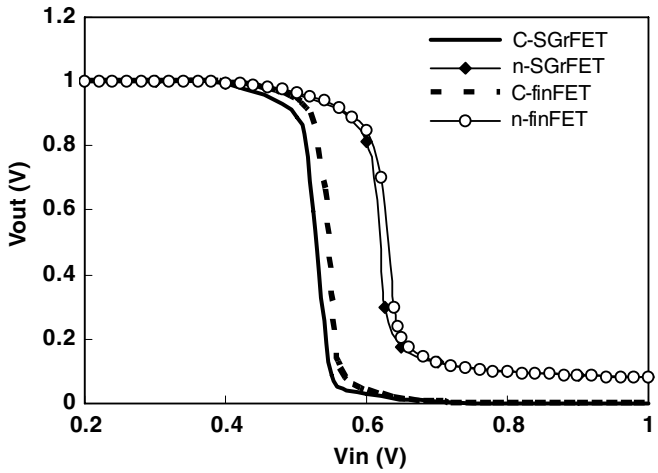


Figure 7. Comparison of the transfer characteristics of the n-SGrFET and C-SGrFET with the n-finFET and C-finFET.

better ON and OFF state performances (similar to standard CMOS technologies) than the n-EDMOS. Power consumed in the C-FET circuit is also lower because current is only drawn when switching [10] while for the n-EDMOS a small current flows for high input voltages on the gate. This current can be reduced by adding an appropriate number of extra fins in parallel for the finFET, but this will substantially increase the area of the inverter. The switching times are given in table 3.

The rise time (t_r) is defined as the time taken for the output voltage to go from 10% to 90% of its final value. The results in table 3 show that the n-SGrFET inverter has very

Table 3. Rise time for the inverter circuits given in figure 6.

Device type	n-SGrFET	C-SGrFET	n-finFET	C-finFET
Rise time (ps)	18.6	85.0	38.5	88.0

fast switching speed compared to both finFET circuits and the C-SGrFET inverter.

The noise margins (NM) of the SGrFET and finFET inverter circuits are extracted following the standard procedure given in [11]. There are two different noise margins for each device [12]:

$$\mathrm{NM}_H = V_{\mathrm{OH}} - V_{\mathrm{IH}} \tag{5}$$

$$\mathrm{NM}_L = V_{\mathrm{IL}} - V_{\mathrm{OL}}, \tag{6}$$

where V_{IL} is the input low voltage, V_{IH} is the input high voltage, V_{OL} is the output low voltage, V_{OH} is the output high voltage and V_{DD} is the supply voltage.

For the SGrFET and finFET $H = 1\ \mathrm{V} = V_{\mathrm{DD}}$ and $L = 0\ \mathrm{V}$. Thus, the input voltage swing is similar to the output voltage swing. The results, summarized in table 4, show a similar noise margin for both device circuits.

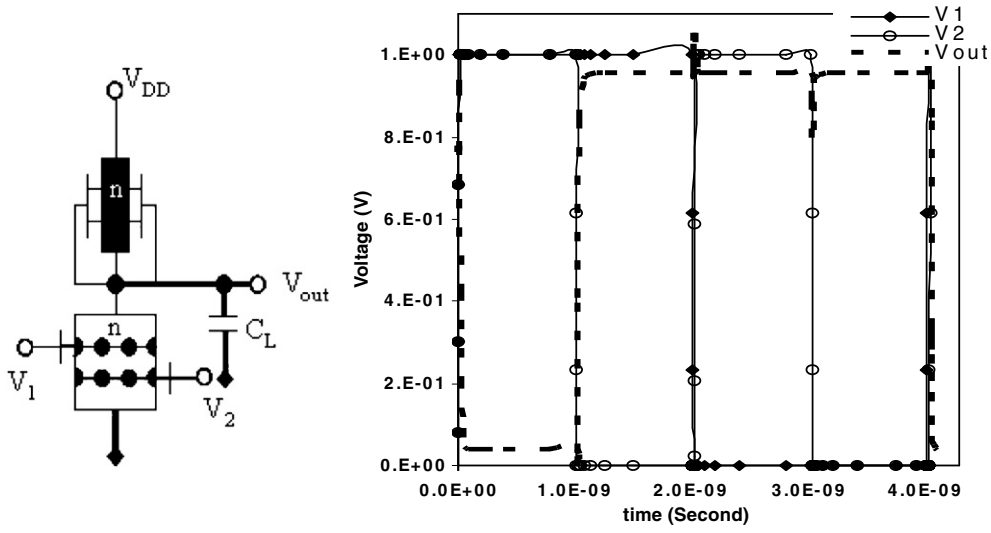
3.2. NAND logic

The multi-gate geometry can be used to minimize the number of devices per logic gate [7, 8, 13]. A two-device NAND can be generated using the split-gate character presented in section 2. Figures 8 and 9 show the circuits and the transient response of the SGrFET and finFET respectively. The circuits are the same, but the SGrFET driver is made of 3 unit cells. As can be seen in figure 6, both n-EDMOS do not switch off completely. Increasing the width of the driver ameliorates this problem but increasing L_c only results in a decrease of device performance (equation (1)). Alternatively, the OFF state can be improved by adding extra unit cells to the SGrFET driver or extra fins to the finFET driver. This increases current drive whilst retaining the other FET parameters. The total width of the SGrFET driver then becomes $W_{\mathrm{tot}} = 3 \times W_{\mathrm{U}} = 3 \times 104\ \mathrm{nm} = 312\ \mathrm{nm}$. Thus, total switch-off comes at a price of increased footprint. The finFETs need three parallel fins in order to achieve a complete OFF state in the output node. The gate input voltages are applied as shown in figure 9 [13, 14].

3.3. NOR logic

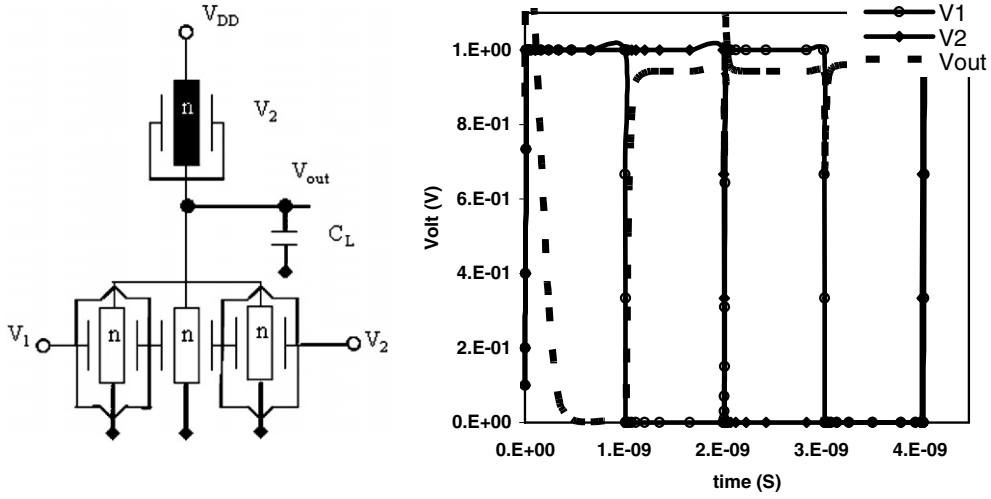
The NOR circuit using SGrFETs consists of an n-type depletion mode follower and a p-type enhancement mode driver. The finFET circuit consists of an n-type enhancement mode driver and n-type depletion mode load [8, 10]. Figures 10 and 11 show the circuits and transient responses of the SGrFET and finFET, respectively. In the SGrFET NOR, the driver takes the split-gate function, whilst the load functions in a single gate contact mode. In the finFET NOR, the driver is a split-gate device and the load a single gate device.

The SGrFET driver has three unit cells and the finFET has three parallel fins in order to achieve a complete high state



(*a*) (*b*)

Figure 8. SGrFETs with a 3-unit cell driver and $V_{G1,2\ max}$ $(=V_{1,\ 2\ man}) = 1$ V. (*a*) NAND circuits and (*b*) transient characteristics. $V_{DD} = 1$ V.



(*a*) (*b*)

Figure 9. FinFETs with a 3-fin driver and $V_{G1,2\ max}(=V_{1,2\ man}) = 1$ V. (*a*) NAND circuits and (*b*) transient characteristics $V_{DD} = 1$ V.

Table 4. Noise margin and main logic levels for all inverter circuits of figure 6.

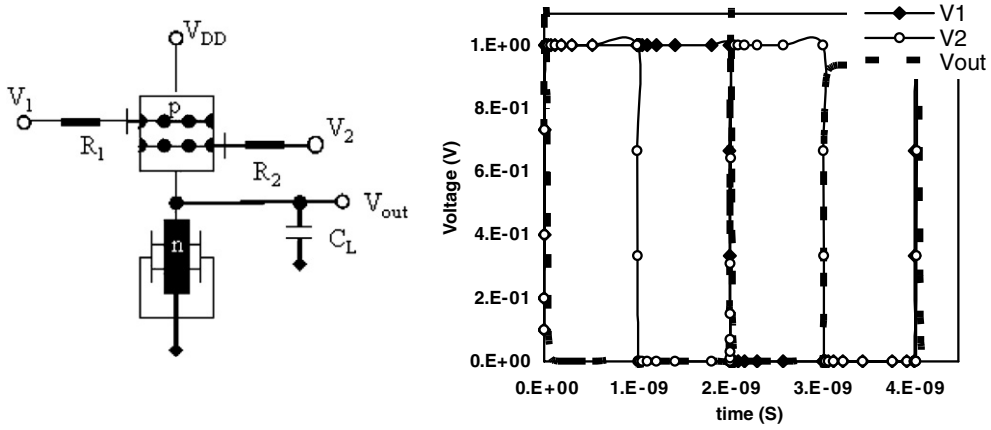
Inverter	V_{OL} (V)	V_{OH} (V)	V_{IL} (V)	V_{IH} (V)	NM_L (V)	NM_H (V)
n-SGrFET	0.16	0.93	0.54	0.66	0.38	0.27
C-SGrFET	0.06	0.97	0.45	0.56	0.39	0.41
n-finFET	0.16	0.94	0.54	0.67	0.38	0.27
C-finFET	0.06	0.97	0.48	0.58	0.42	0.39

in the output node. For convergence reasons in the SGrFET simulations, the input voltages are connected via resistors R_1 and R_2 which have no further impact on the results. The input voltage swings between 0 V and 1 V for both SGrFET and finFET circuits.

3.4. XOR logic

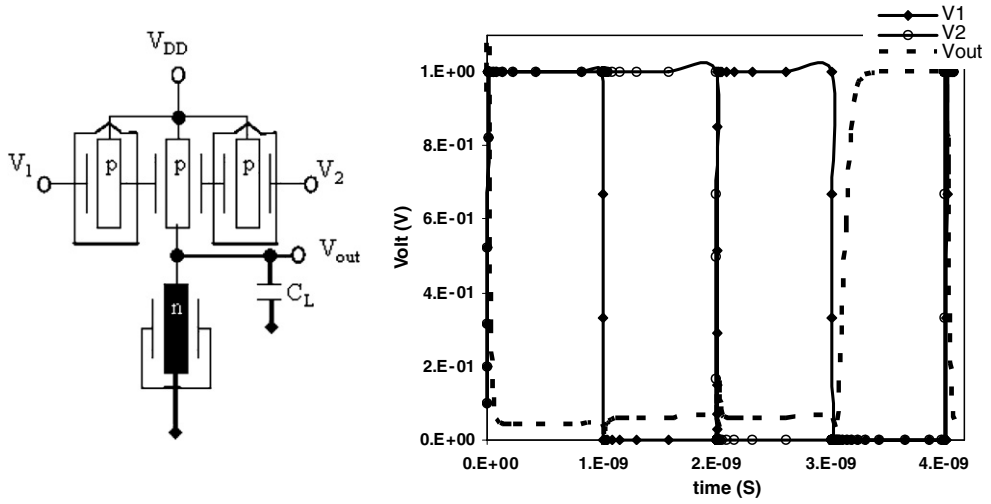
The XOR circuit is similar to the n-EDMOS circuit. To construct an XOR, four inputs are required. This can be accomplished with the SGrFET as 1-unit cell has four gate fingers, and each finger can be biased independently. In order to ensure complete switch-off, a 3-unit cell driver is used. The XOR circuit and transient response are given in figure 12.

Figure 13 shows the finFET-based circuit and the transient response [8, 10]. The circuit consists of four independent gate devices as drivers and a single contact gate device as load. Unlike for the SGrFET XOR, the output of the finFET XOR does not go to completely OFF. A further increase in the number of fins does not solve the problem. The poor



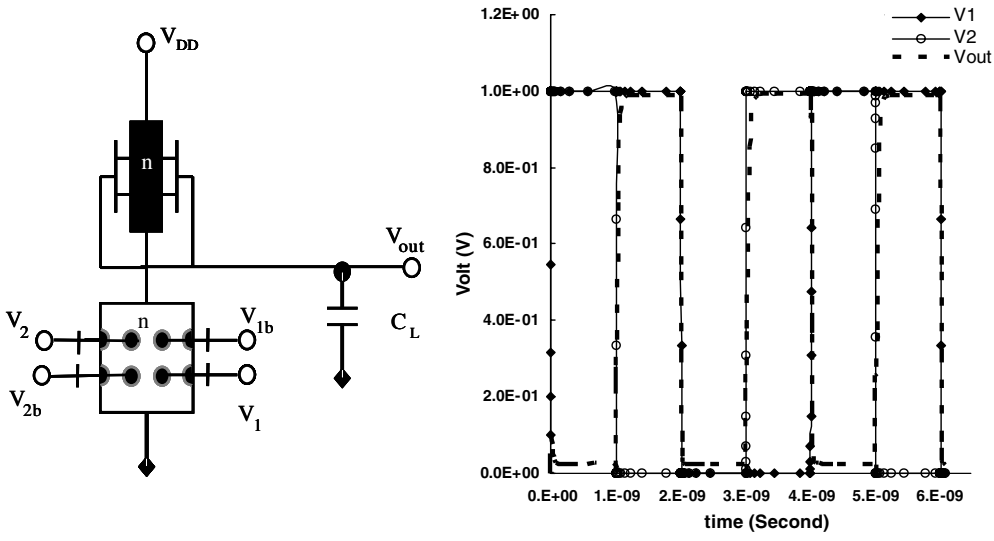
(*a*) (*b*)

Figure 10. (*a*) SGrFET NOR circuit, (*b*) transient response with $V_{G1,2\ max}(=V_{1,\ 2\ man}) = 1$ V. $V_{DD} = 1$ V.



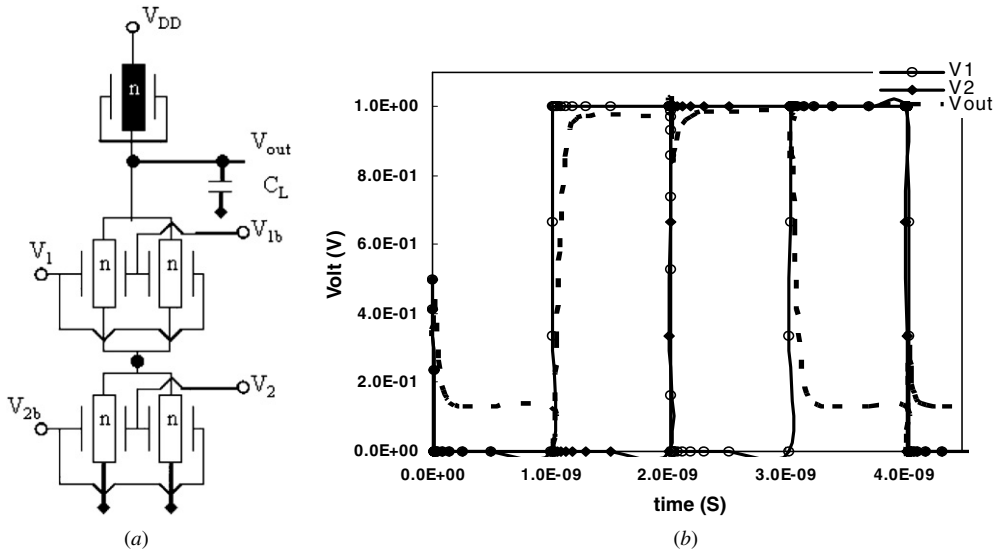
(*a*) (*b*)

Figure 11. (*a*) FinFET NOR circuit, (*b*) transient response with $V_{G1,2\ max}(=V_{1,2\ man}) = 1$ V. $V_{DD} = 1$ V.



(*a*) (*b*)

Figure 12. (*a*) SGrFET XOR circuit. (*b*) Transient response. $V_{ib} = \overline{V_i}(=V_{Gib})$.



(*a*) (*b*)

Figure 13. (*a*) FinFET XOR circuit. (*b*) Transient response. $V_{ib} = \overline{V_i}(=V_{Gib})$.

Table 5. ON and OFF states for both finFET and SGrFET working in the enhancement mode, $I_{N,P}$ denotes an n-, p-type device.

V_{in} (V)	$I_{N\text{-SGrFET}}$ (A μm^{-2})	$I_{P\text{-SGrFET}}$ (A μm^{-2})	$I_{N\text{- finFET}}$ (A μm^{-2})	$I_{P\text{-finFET}}$ (A μm^{-2})
$V_{ON} = V_{DD} = 1$ V	2.1×10^{-4}	-1.9×10^{-4}	4.6×10^{-4}	-3.9×10^{-4}
$V_{OFF} = 0$	8.0×10^{-13}	-1.3×10^{-10}	1.5×10^{-12}	-2.2×10^{-10}

performance of the finFET XOR circuit is potentially due to the unstable circuit node where the source and drain electrodes of two drivers are connected.

4. Discussion and conclusions

We analyzed the dc and transient performance of both SGrFET and finFET logic circuits, based on the use of independent gating, via TCAD simulations. For this comparison, the distance between two gates on both sides of the fin and the distance between the gating cylinders in one row of the SGrFET are taken equal. The other geometrical parameters are the same for both devices. The switching speed of the all-n-SGrFET inverter was found to be more than ten times faster than the n-finFET inverter. The C-finFET is slightly faster than the C-SGrFET. The n-FET inverters consume more power than the C-FET for both device types.

The NAND and NOR circuits can be constructed with only two devices for both SGrFET and finFET. Complete off-switching can be obtained for the SGrFET circuits by using multiple unit cells; this approach does not hinder the split-gate option. The parallel fin approach for the finFET is used when the split-gate configuration needs to be retained. Therefore, the driver in the finFET needs to be constructed with increased fin width. The XOR circuit can be implemented with only two SGrFETs while four finFETs are required.

The SGrFET logic is faster than the finFET one. This result is due to the higher mobility of carriers in the SGrFET than the finFET and the use of multiple unit cell configuration of the SGrFET.

To estimate the static power dissipation, we use a simple approach [11]:

$$\text{Peak power dissipation: } P_{peak} = V_{DD} \times I_{sat}$$
$$\text{OFF power dissipation: } P_{OFF} = V_{DD} \times I_{OFF}.$$

Table 5 gives the ON and OFF currents in all devices when taking ON = 1 V and OFF = 0 V. ON currents in finFETs are higher than in SGrFETs and thus cause more power consumption. OFF currents in finFETs are also higher and thus the stand-by power consumption will be higher. These results imply that the SGrFET can deliver faster switching in its split-gate logic configuration for reduced power consumption than its finFET counterpart with the same geometrical dimensions.

These simulation results demonstrate the potential advantage of using a SGrFET for logic applications.

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